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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,592	12/05/2003	Gary L. Swoboda	TI-34662	1553
23494	7590	09/13/2006	EXAMINER	
TEXAS INSTRUMENTS INCORPORATED P O BOX 655474, M/S 3999 DALLAS, TX 75265			RIZK, SAMIR WADIE	
			ART UNIT	PAPER NUMBER
			2133	

DATE MAILED: 09/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/729,592	SWOBODA ET AL.
	Examiner	Art Unit
	Sam Rizk	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 05 December 2003.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-20 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 05 December 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTIONS

- Claims 1-20 have been submitted for examination
- Claims 1-20 have been rejected

Drawings

1. Figures 1A and 1B should be designated by a legend such as --Background Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claim 12 is directed to non-statutory subject matter. Claim 12 is a series of steps of:
- determining when a first and a second input signal group meets at least one predetermined condition.

Comparing two signals are non-statutory, the results of the process must produce useful and tangible outcome.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Swaine et al. US publication no. 2002/0184477 (Hereinafter Swaine).

4. In regard to claim 1, Swaine teaches:

- A comparator unit comprising:
 - a first comparator responsive to a first signal group, the first comparator determining when a first predetermined relation is present to a first reference signal group;
 - a second comparator responsive to a second signal group, the second comparator determining when a second predetermined relation is present to a second reference signal group; and
 - a second inter-comparator conductor, the second inter-comparator conductor applying an indicia of an identification of the second predetermined condition to first comparator, the first comparator generating an event signal when the first and the second predetermined conditions are identified.

(Note: Sections [0022] and [0029] in Swaine)

5. In regard to claim 2, Swaine teaches:

- The comparator unit as recited in claim 1 wherein the first and the second signal groups are the same.

(Note: Section [0052], line 7 in Swaine)

6. In regard to claim 3, Swaine teaches:

- The comparator unit as recited in claim 1 wherein the first and second signal groups are address signal groups.

(Note: Section [0051], line 4 in Swaine)

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7. In regard to claim 4, Swaine teaches:

- The comparator unit as recited in claim 1 wherein the first and the second signal groups are same address signal group.

(Note: Section [0052], line 7 in Swaine)

8. In regard to claim 5, Swaine teaches:

- The comparator unit as recited in claim 1 wherein either one of the first and the second comparator can generate an event signal when at least one of a touching requirement and an exact requirement is satisfied by an applied address signal group.

(Note: Section [0061] in Swaine)

9. In regard to claim 6, Swaine teaches:

- A comparator unit comprising:
- a first comparator and a second comparator, each comparator including:
 - a comparison logic unit for comparing an input signal group with a predetermined condition is identified; and
 - an event signal generating unit, the comparison logic unit applying a signal to the event generator unit and to the event signal generating unit of the other comparator when the predetermined condition is identified, the event generating unit generating an event signal when the signals from the two comparator logics have predetermined values.

(Note: Any of figures 3-6 in Swaine)

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10. In regard to claim 7, Swaine teaches:

- The comparator unit as recited in claim 6 wherein each comparator includes a data qualifying unit, the data qualifying unit responsive to an input signal, the input signal determining when a preestablished signal group has certain characteristics, the data qualifying unit applying a control signal to the comparison logic unit determining whether generation of an event signal is enabled.

(Note: Section [0052] in Swaine)

11. Claim 8 is rejected for the same reasons as per claim 3.

12. Claim 9 is rejected for the same reasons as per claim 4.

13. In regard to claim 10, Swaine teaches:

- The comparator unit as recited in claim 6 wherein the predetermined conditions are entered in the comparator logic by control signals.

(Note: FIG. 2, reference sign (120) in Swaine)

14. In regard to claim 11, Swaine teaches:

- The comparator as recited in claim 10 wherein each comparator can operate independently, each comparator capable of generating an event signal in response to at least one of a touching requirement and an exact requirement.

(Note: Section [0053] in Swaine)

15. In regard to claim 12, Swaine teaches:

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- The method of determining when a first and a second input signal group meets at least one predetermined condition, the method comprising:
 - determining in a first comparator when the first input signal group meets a first predetermined condition; determining in a second comparator when the second input signal group meets a second predetermined condition; and
 - generating an output signal when the first and the second predetermined conditions are met.

(Note: Claim 17, item (ii) in Swaine)

16. Claim 13 is rejected for the same reasons as per claim 3.
17. Claim 14 is rejected for the same reasons as per claim 4
18. Claim 15 is rejected for the same reasons as per claim 5.
19. Claim 16 is rejected for the same reasons as per claim 7.
20. In regard to claim 17, Swaine teaches;
 - In a target processor, apparatus for generating a trigger signal, the apparatus comprising:
 - a plurality of event signal generating units, wherein at least one signal generating unit is a comparator unit, the comparator unit including:
 - a first comparator and a second comparator, each comparator having:
 - a comparison logic unit for comparing an input signal group with a predetermined condition is identified; and

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- an event signal comparison logic unit applying a generating unit, the signal to the event generator unit and to the event signal generating unit of the other comparator when the predetermined condition is identified, the event generating unit generating an event signal when the signals from the two comparator logics have predetermined values.
- a trigger generation unit coupled to the plurality of event signal generation units, the trigger generation unit responsive to at least one preselected event signal for generating an associated trigger signal, the trigger generating unit generating a trigger control signal;

(Note: FIG. 2, and section [0048] in Swaine)

21. Claim 18 is rejected for the same reasons as per claim 3.
22. Claim 19 is rejected for the same reasons as per claim 4.
23. Claim 20 is rejected for the same reasons as per claim 5.

Conclusion

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
 - Ranson et al. US patent no. 5887003 teaches apparatus and method for comparing a group of binary fields with an expected pattern to generate match results.
 - Whitsel et al. US patent no. 5640542 teaches on-chip in-circuit-emulator memory mapping and breakpoint register modules.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronics Business Center (EBC) at 866-217-9197 (toll-free)

Sam Rizk, MSEE, ABD

Examiner

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[Handwritten signature of Sam Rizk]
9/6/06
JOSEPH TORRES
PRIMARY EXAMINER